Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1(previously presented) A damascene process capable of avoiding via resist poisoning, the damascene process comprising:

providing a semiconductor substrate with a low-k dielectric layer (k≦ 2.9) thereon, a SiC layer over the low-k dielectric layer, a metal layer over the SiC layer, and a first bottom anti-reflection coating (BARC) layer over the metal layer;

forming a first resist layer on the first BARC layer, wherein the first resist layer has a trench opening to expose a portion of the first BARC layer;

etching through the first BARC layer and the metal layer and etching a portion of the SiC layer to form a trench structure in the SiC layer;

removing the first resist layer and the first BARC layer;

forming a blocking layer on the surface of the trench structure of the SiC layer, wherein the blocking layer is used to prevent unpolymerized precursors diffused out from the low-k dielectric layer from contacting an overlying resist;

forming a second BARC layer on the blocking layer, the second BARC layer filling the trench structure;

forming a second resist layer on the second BARC layer, the second resist layer having a via opening to expose a portion of the second BARC layer;

etching through the second BARC layer ,the SiC layer, and the blocking layer, and etching a portion of the low-k dielectric layer

to form a via structure in the low-k dielectric layer;

removing the second resist layer and the second BARC layer; and

performing a dual damascene process using the metal layer and the SiC layer as masks to make the low-k dielectric layer form a dual damascene structure having the trench and the via structure.

Claim 2 (original) The process of claim 1 wherein the blocking layer is formed by Ar plasma hitting the SiC layer.

Claim 3 (previously presented) The process of claim 2 wherein the Ar plasma comprises a fluorine substance.

Claim 4 (previously presented) The process of claim 3 wherein the fluorine substance is CF_4.

Claim 5 (original) The process of claim 1 wherein the low-k dielectric layer comprises a carbon-doped oxide (CDO) substance.

Claim 6 (original) The process of claim 1 wherein a dielectric layer is set between the metal layer and the first BARC layer.

Claim 7 (original) The process of claim 1 wherein the thickness of the SiC layer is less than 700 angstroms.

Claim 8 (currently amended) A damascene process capable of avoiding via resist poisoning, the damascene process comprising:

providing a semiconductor substrate with a low-k dielectric layer ($k \leq 2.9$) thereon, and a SiC layer over the low-k dielectric layer;

forming a blocking layer on the SiC layer, wherein the blocking layer is formed by Ar plasma comprising fluorine substance hitting the SiC layer and is used to prevent unpolymerized precursors diffused out from the low-k dielectric layer from contacting an overlying resist;

forming a BARC layer on the blocking layer;

forming a resist layer on the BARC layer, wherein the resist layer has a via opening to expose a portion of the BARC layer; and

etching through the BARC layer, the blocking layer, and the SiC layer, and etching a portion of the low-k dielectric layer to form a single damascene structure in the low-k dielectric layer.

Claims 9-10 (cancelled)

Claim 11 (currently amended) The process of claim [[10]]8 wherein the fluorine substance is CF_4.

Claim 12 (original) The process of claim 8 wherein the low-k dielectric layer comprises a carbon-doped oxide substance.

Claim 13 (currently amended) The process of claim [[1]]8 wherein the thickness of the SiC layer is less than 700 angstroms.